Silicon Tracker Design

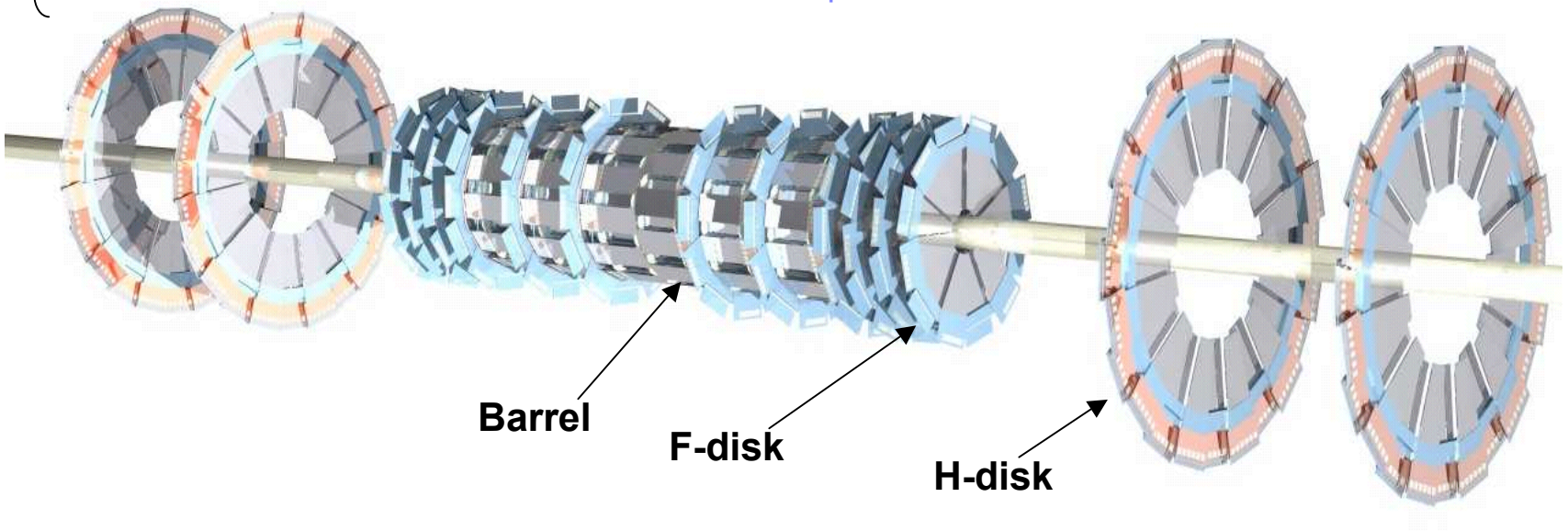
Hybrid system: **barrel detectors measuring primarily r-ϕ of vertices for low η tracks, disk detectors measuring r-z as well as r-ϕ of vertices for high η tracks (3D)**

- disk separation must be kept small to minimize extrapolation errors
- each plane of disks also represents a dead region (~8 mm gap) between the barrels which lowers overall efficiency of the detector ⇨ compromise!!!!!

General characteristics

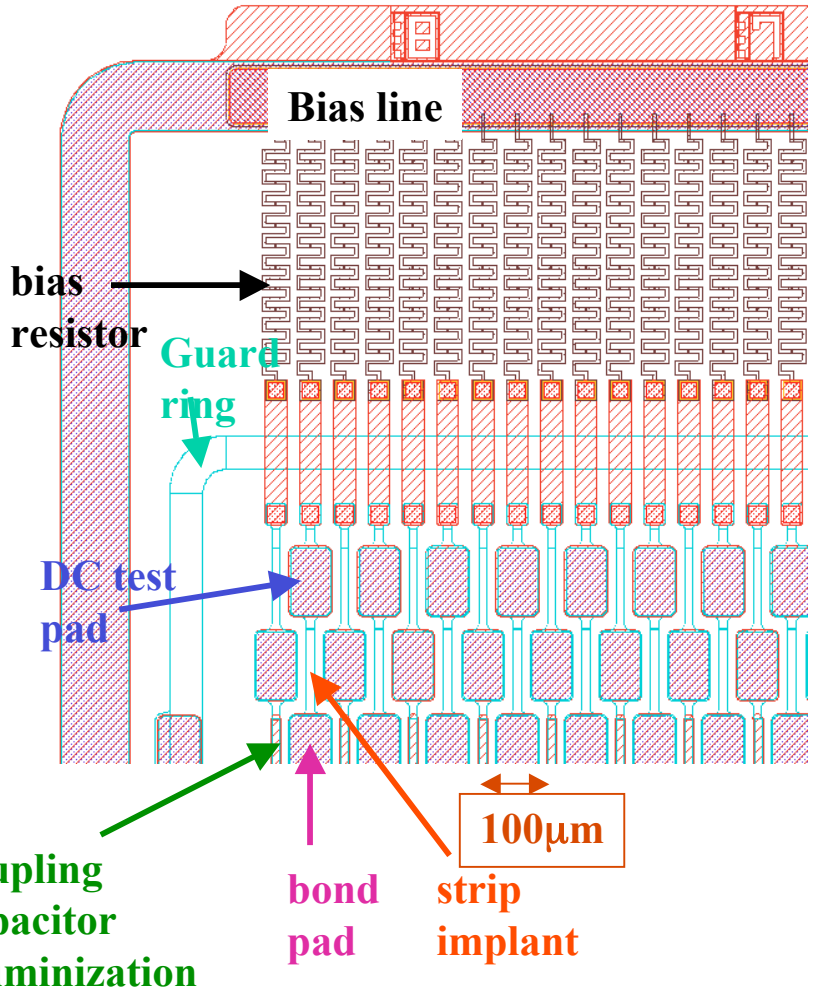
- 3D track reconstruction capabilities,
- good acceptance for high p_T tracks (top decay,…),
- six 12cm long barrels (four detector layers) with interspersed disks (F-disks) for forward tracking,
- external large area disks (H-disks) for forward tracking ($2 < |\eta| < 3$),
- detectors and inboard electronics radiation hard up to 1 MRad

- axial hit resolution: ~ 10 μm
- *z* hit resolution:
  ~ 35 μm for 90^0 stereo
  ~ 450 μm for 2^0 stereo

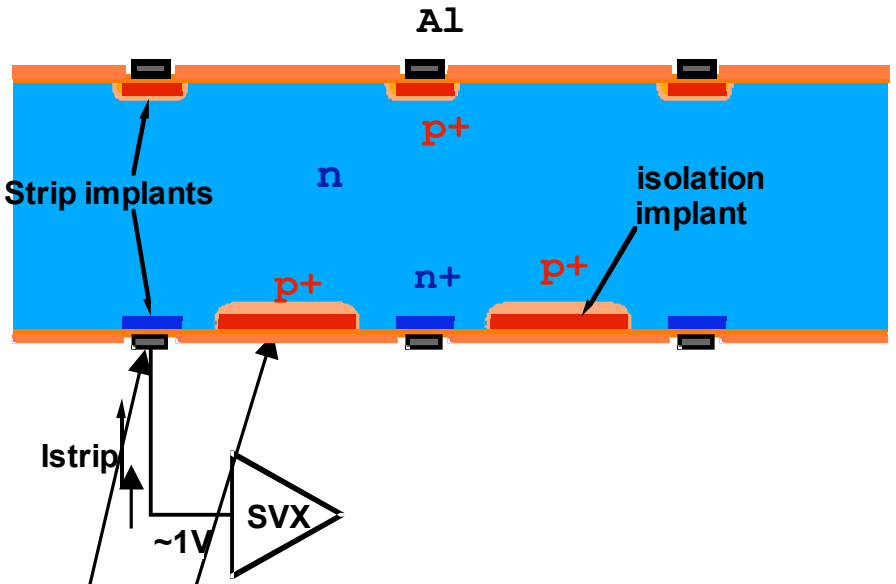


Silicon Detectors

Single sided devices



Double sided devices



AC-coupling: add thin (2500Å) SiO_2 layer between readout implant and Al (integrated capacitor).

⇒ Immunity to DC reverse currents caused by radiation.

Capacitors must withstand bias voltage.

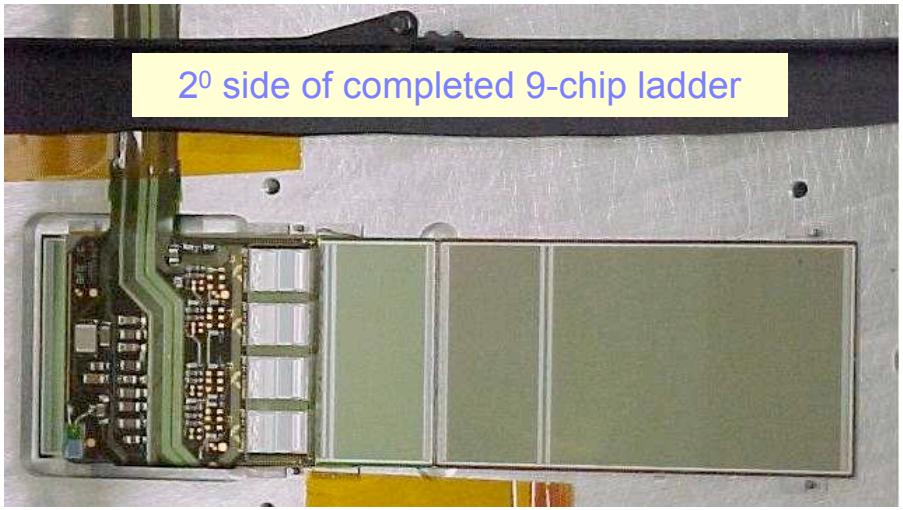
p-stop: add blocking p+ strips on n-side to ensure strip isolation at full depletion

Silicon Detectors

D0	Barrels	F-Disks	H-Disks
Layers/planes	4	12	4
Channels	387120	258000	147456
Modules	432	144	192
Readout Length	12 cm	7.5 cm	14.6 cm
Inner Radius	2.7 cm	2.6 cm	9.5 cm
Outer Radius	9.4 cm	10.5 cm	26 cm

~ 793,000 readout channels

Intermediate in size between previous generation of collider detectors and LHC



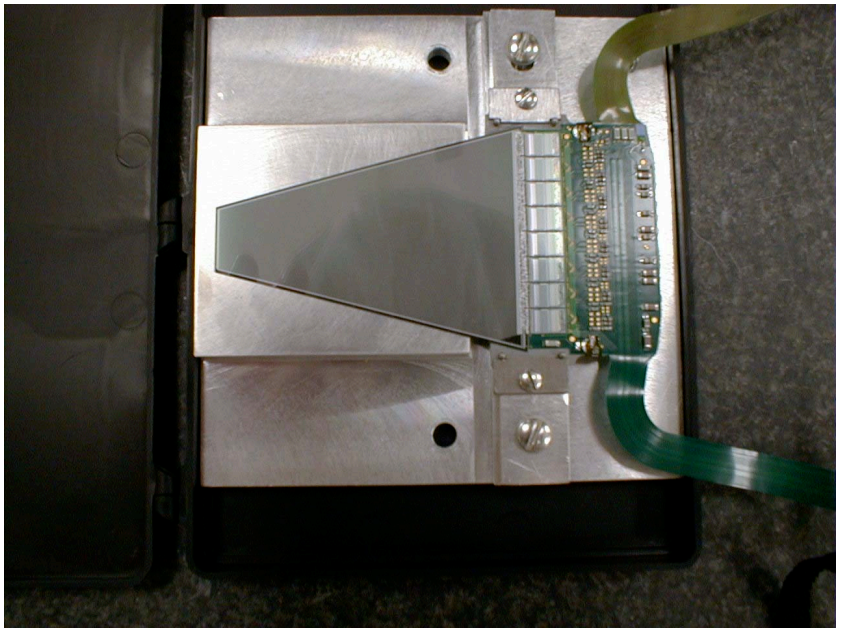
- **Barrel Detectors**
  - Single sided ladders (144)
    - AC coupled
    - 50 μm (p-side) pitch
    - Layers 2 and 4 of two outer barrels
  - Double sided ladders

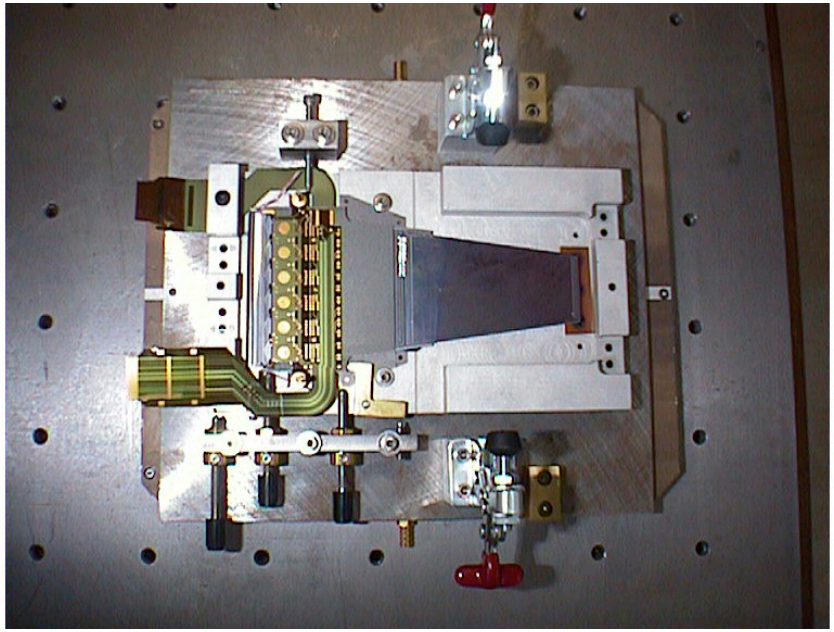
    2^0 stereo ladders (432)
    - AC coupled
    - 50 μm (p-side), 62.5 μm (n-side) pitch
    - Layers 2 and 4

    90^0 stereo ladders (144)
    - AC coupled
    - Double metal in 6" technology
    - 50 μm (p-side), 153 μm (n-side) pitch
    - Layers 1 and 3 of four inner barrels

- **Disk Detectors**

  - F-Wedge Detectors (144) ⇒ Central Disks
    - 2.6 cm < r < 10 cm
    - AC coupled
    - Double sided wedges with ±15^0 (30^0 effective stereo)
    - 50 μm (p-side), 62.5 μm (n-side) pitch
    - Variable strip length

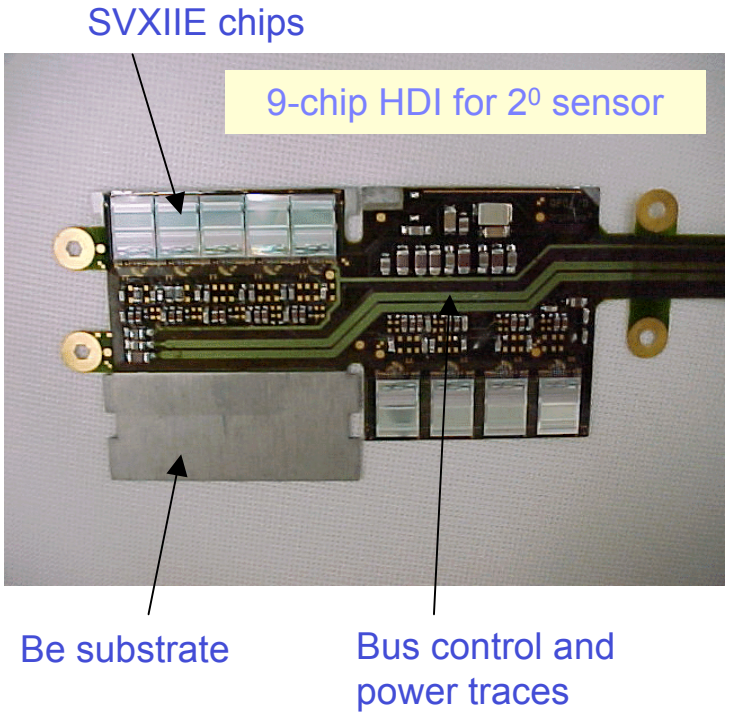




  - H-Wedge Detectors (384) ⇒ Forward Disks
    - 9.6 cm < r < 23.6 cm
    - AC coupled
    - Single sided glued back-to-back with ±7.5^0 (15^0 effective stereo)
    - 40 μm (p-side) strip pitch, 80 μm readout pitch
    - Variable strip length

High Density Interconnect

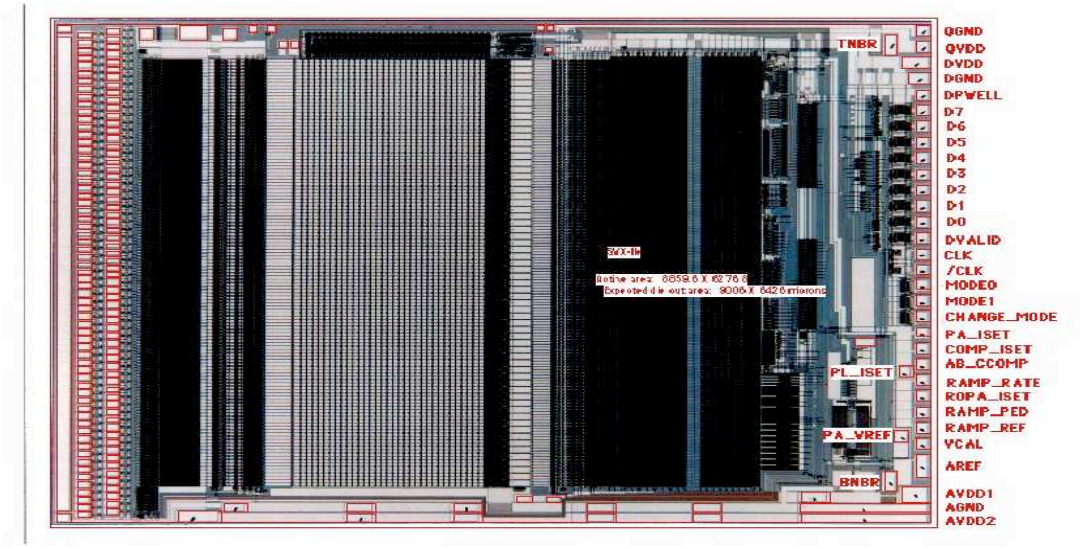
- Barrel/disk geometry with 2mm gap forces to move electronics and cables inboard
  - ⇨ flexible HDI tails
- Kapton based flex circuits, double sided with 0.2 mm pitch, for chip mounting
- Laminated to Be substrate and glued to Si sensor
- Connects Si to SVX chip and SVX chip to flex circuit though wirebonds
- Connects to *low-mass cable* which carries signals out of the detector

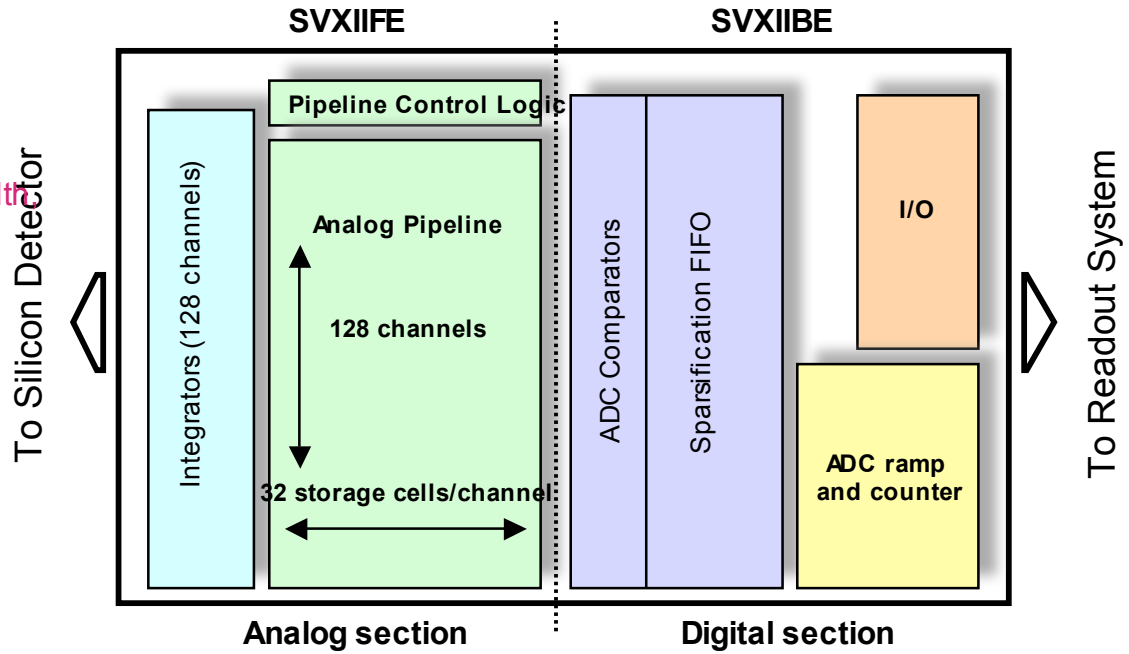


SVXIIe chip

- 1.2 μm CMOS amplifier/analog delay/ADC chip fabricated in the UTMC rad hard process
- LBL/Fermilab group (Milgrome/Yarema)

- Features:
  - 128 channels (5 mW/channel)
  - 32 cell pipeline /channel
  - 8-bit Wilkinson ADC with sparsification /channel
  - Programmable test pattern, ADC ramp+pedestal, preamp bandwidth, calibration, polarity…
  - 53 MHz readout
    106 MHz digitization
  - Dimensions: ~ 6.4 x 9.7 mm^2
  - ~ 85,000 transistors





SVXIIe chip

- Can be externally programmed to achieve optimal performance for any interaction rate (132/396 ns) and detector capacitance from 10 to 35 pF (*preamp bandwidth adjustment*)

- Chip noise:

  490 e + 50 e/pF (τ=200ns)

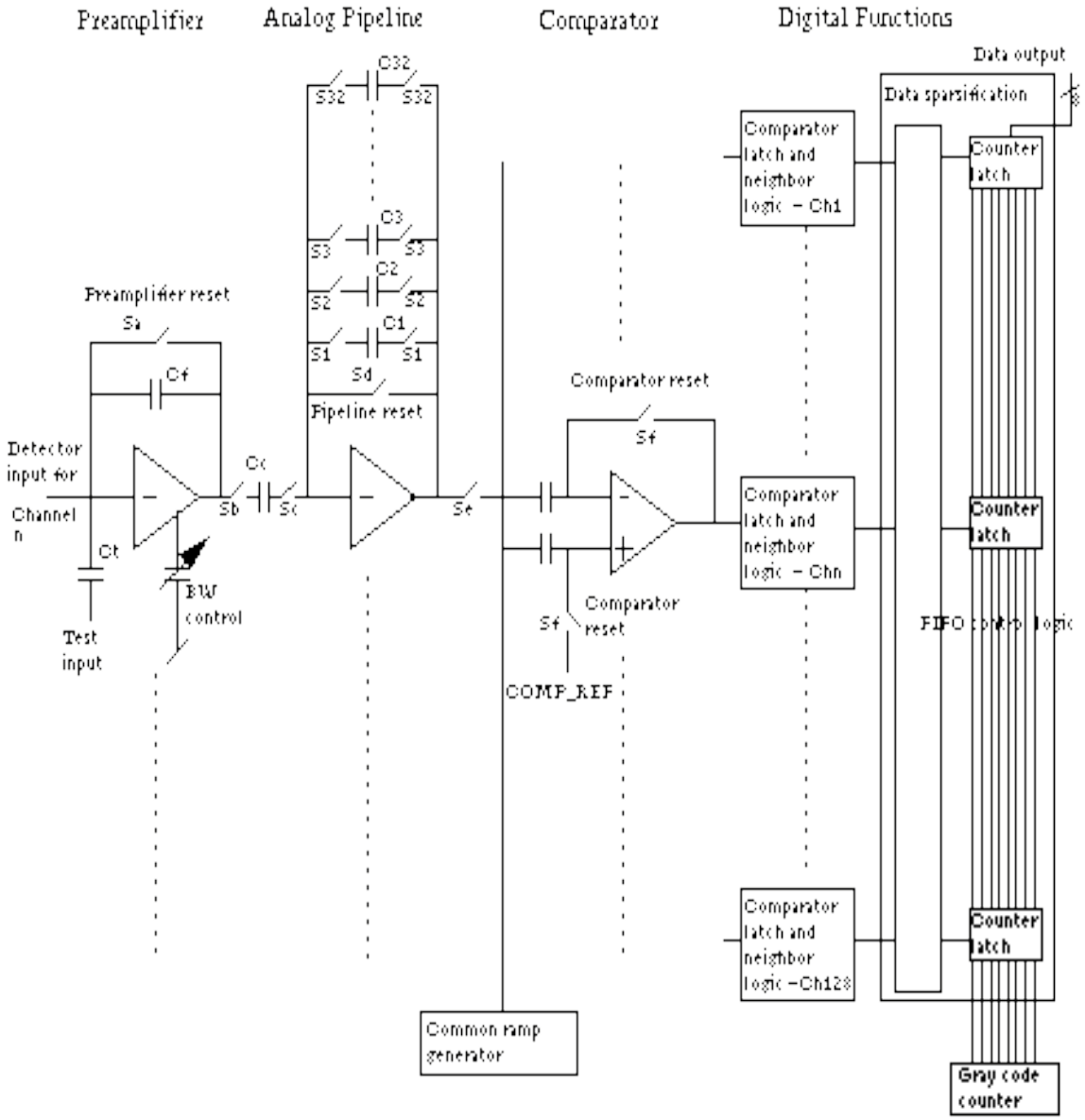
  ~1200 e ENC for C_{det} = 15 pF

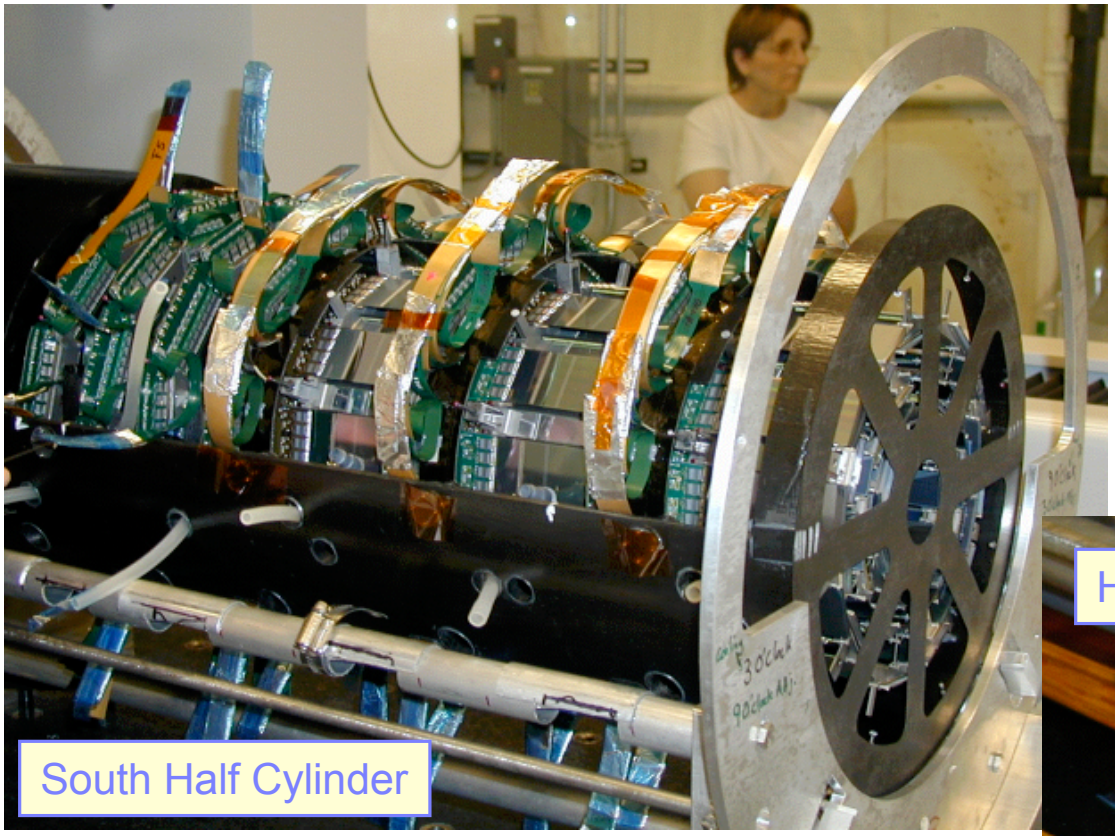
  1 mip ~4 fC ~ 25,000 e

  S/N ~ 21

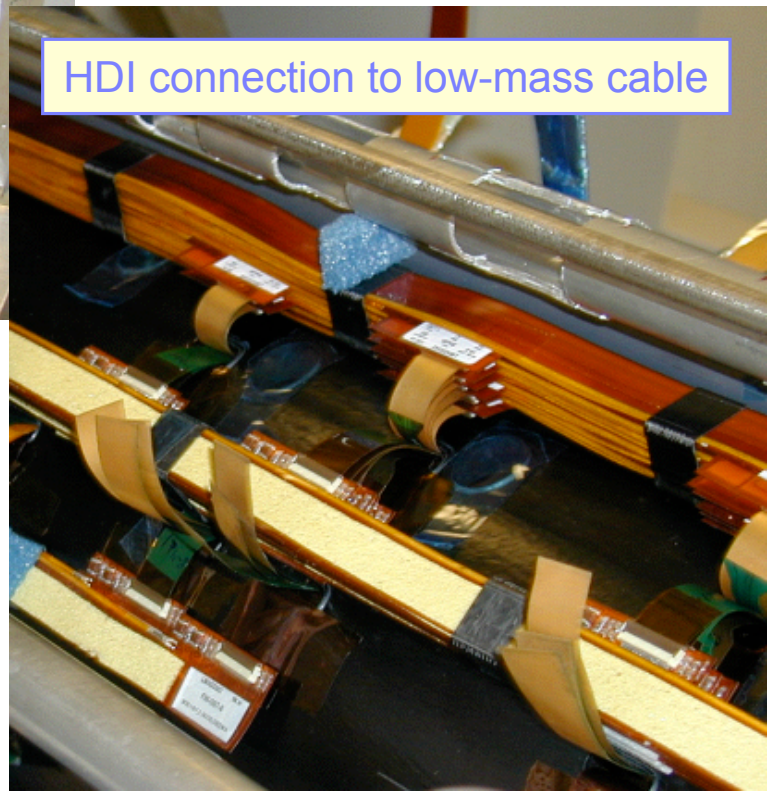
- Maximum programmable delay in analog pipeline:

  32 x 132 ns = **4.2 μs**

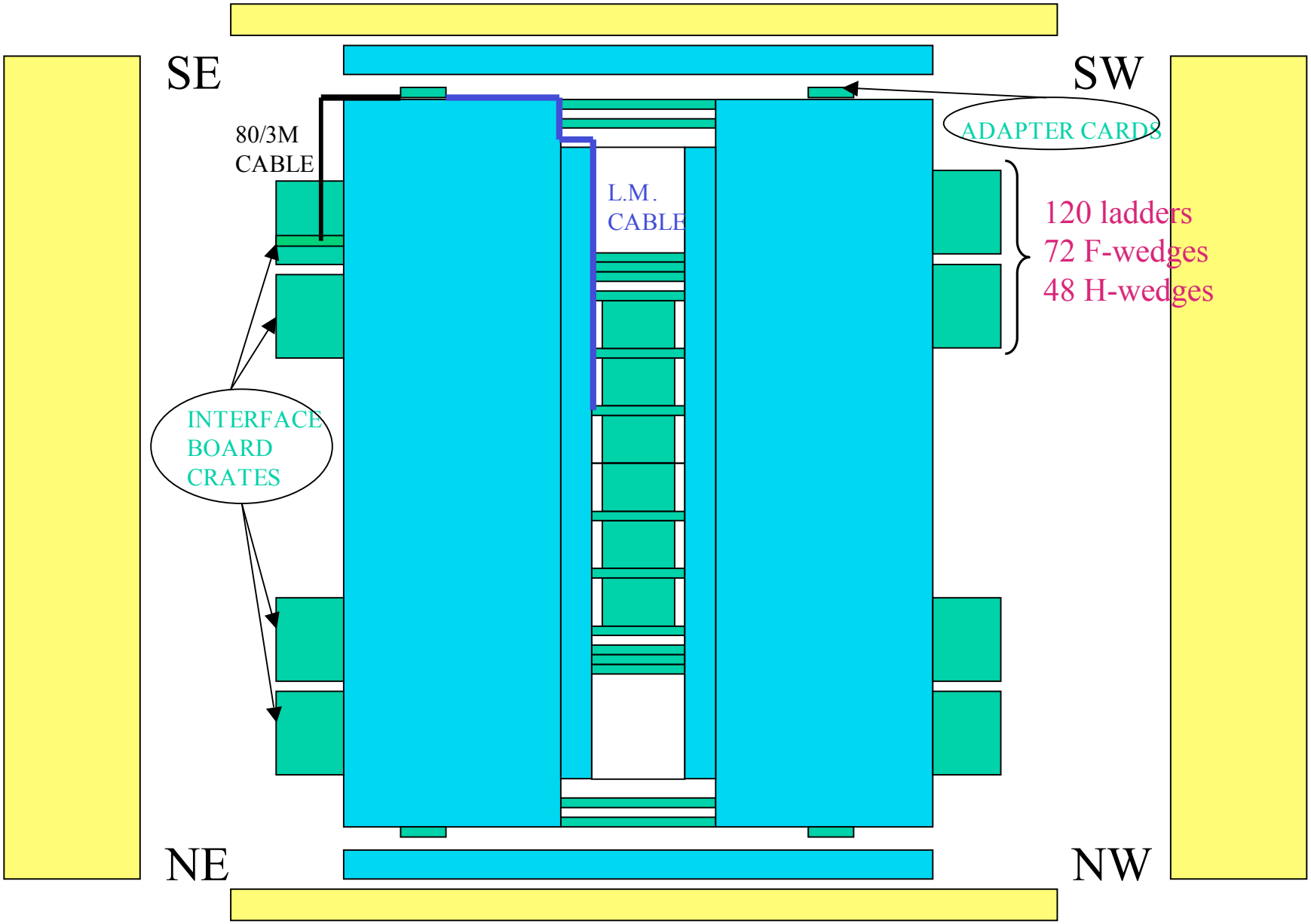


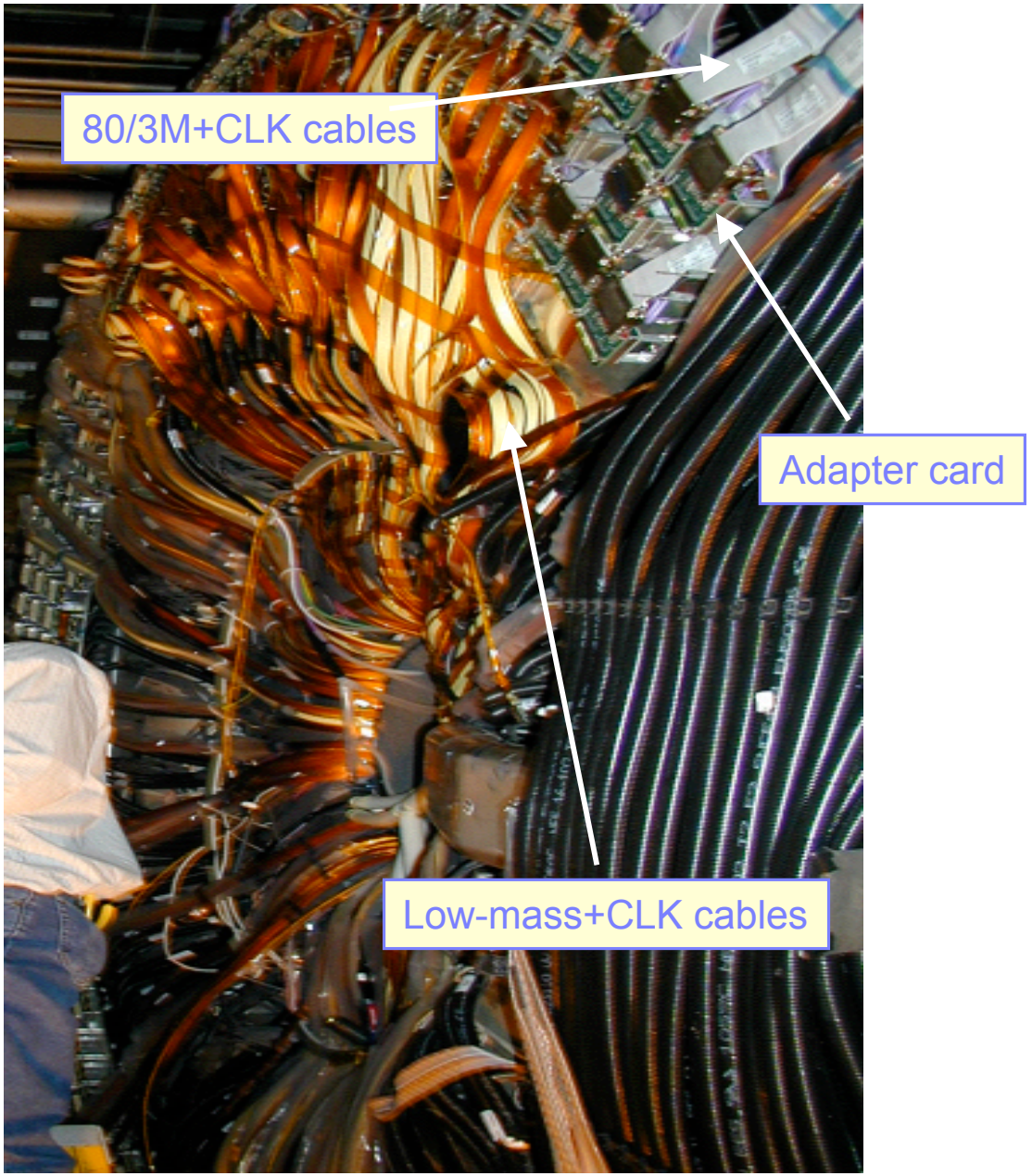


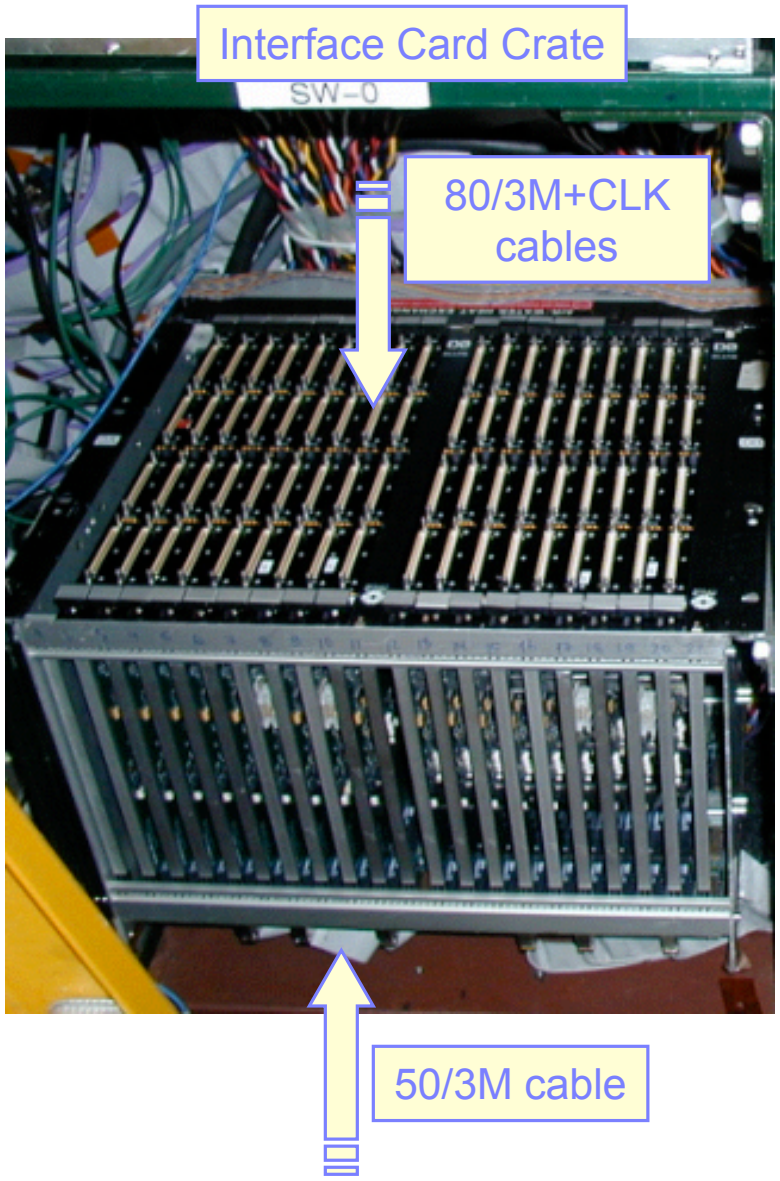
South Half Cylinder



HDI connection to low-mass cable

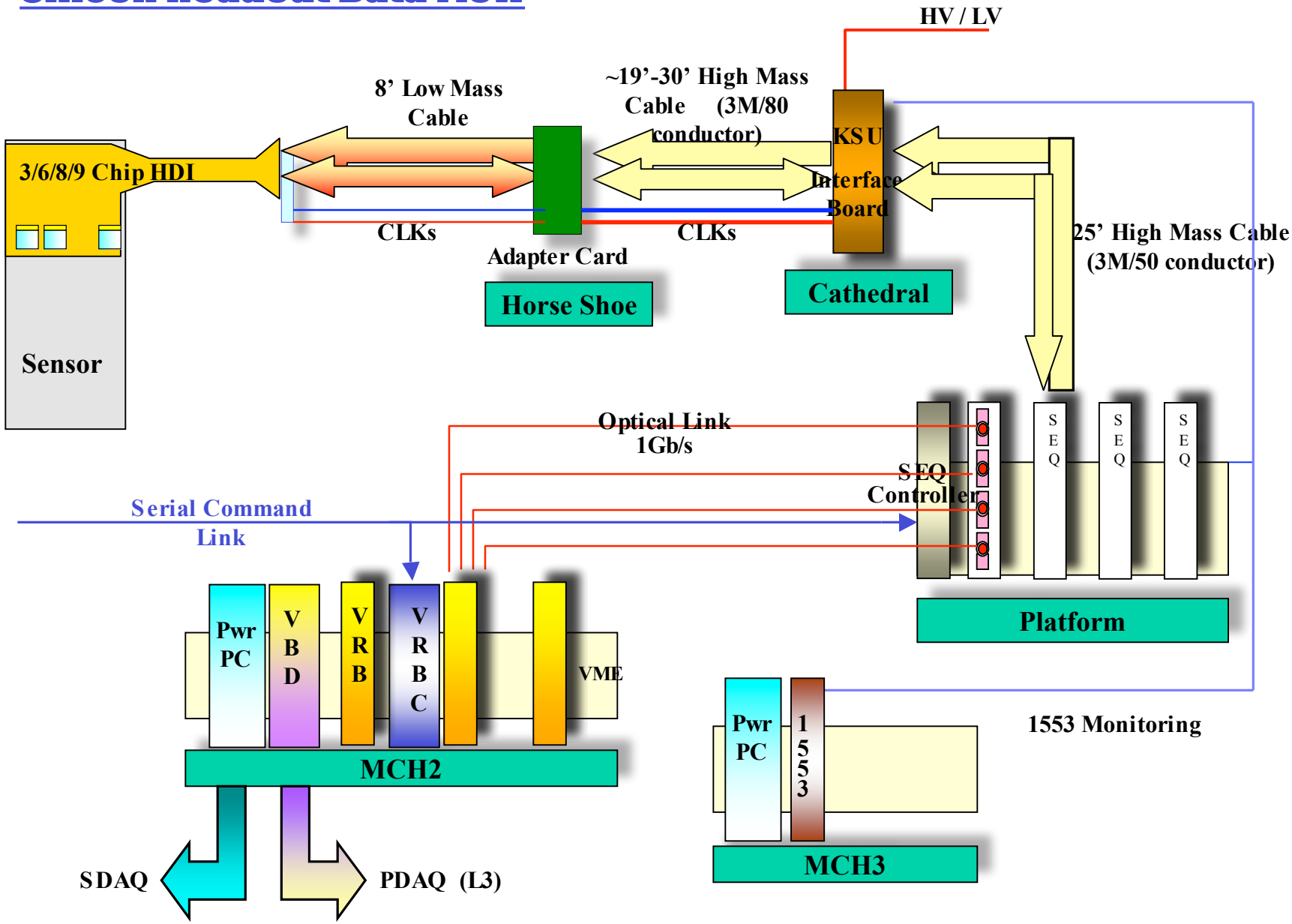

SE
SW
NE
NW
80/3M
CABLE
L.M.
CABLE
ADAPTER CARDS
120 ladders
72 F-wedges
48 H-wedges
INTERFACE
BOARD
CRATES


80/3M+CLK cables
Adapter card
Low-mass+CLK cables


Interface Card Crate
80/3M+CLK cables
50/3M cable


Fuse Panel
LV Power Supplies
Interface Card Crate

Silicon Readout Data Flow

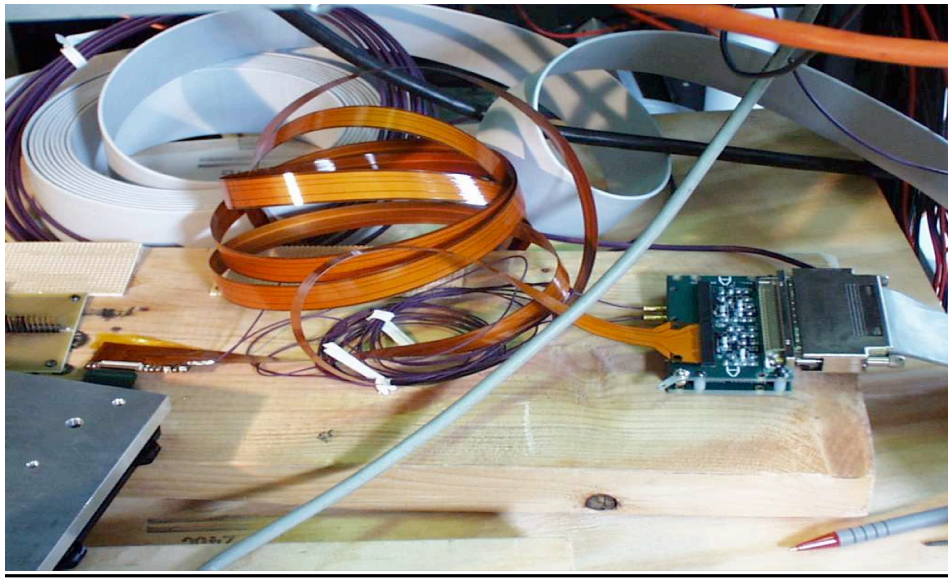


Individual Readout Components

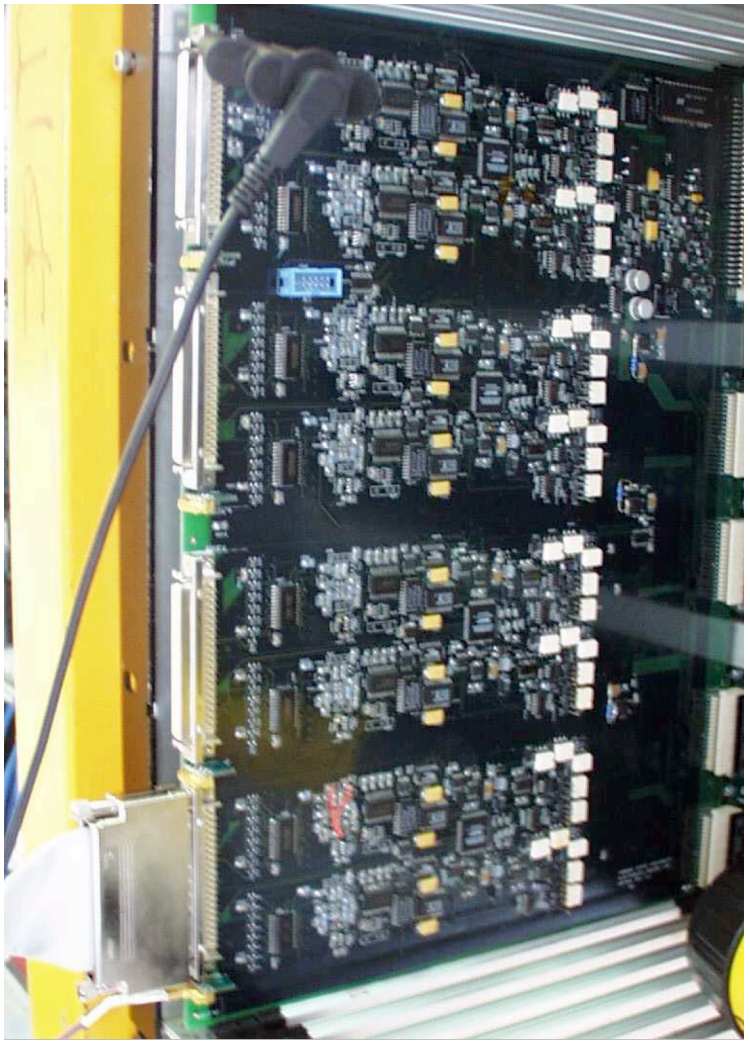
INTERFACE CARD

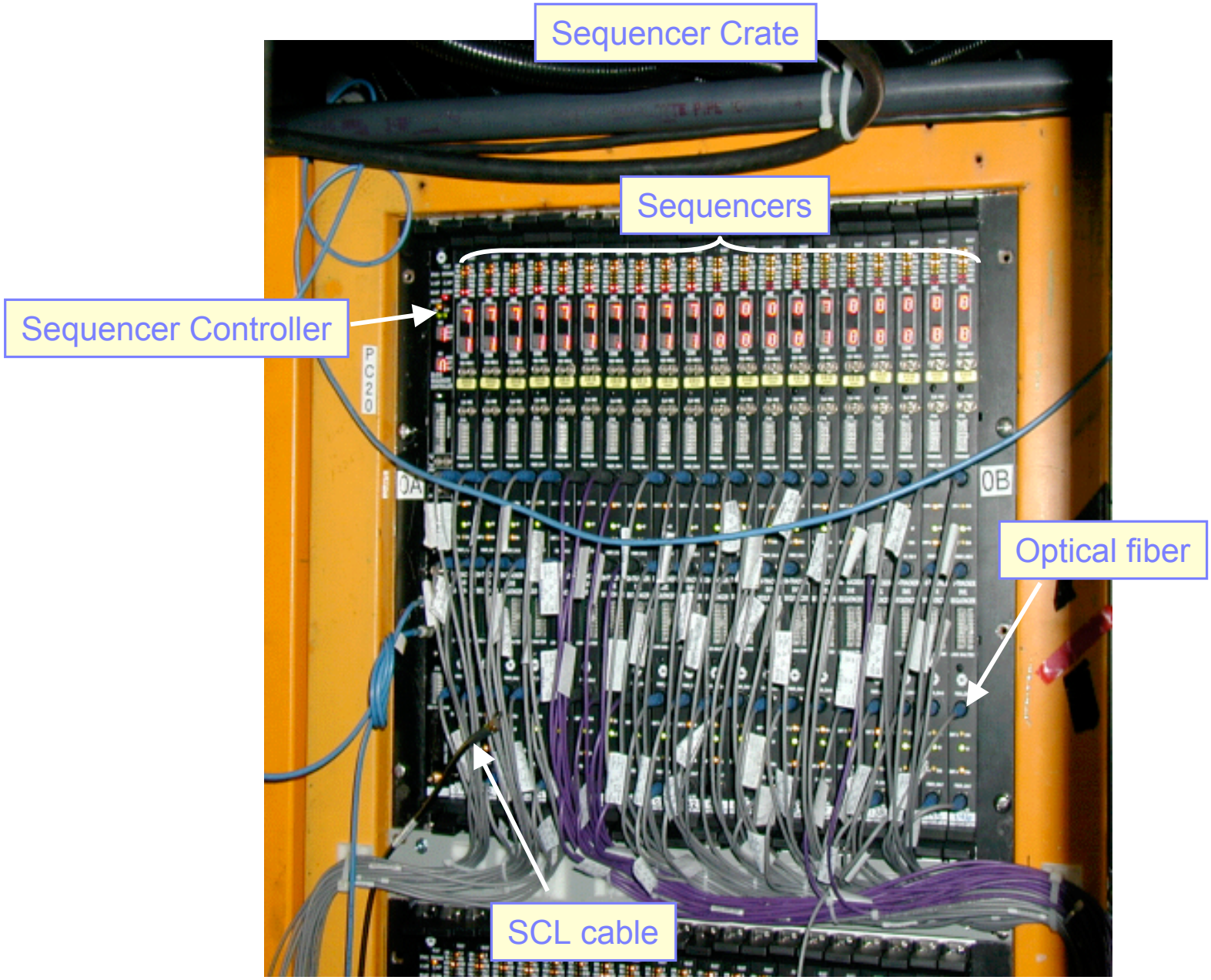
- **8 crates (2/quadrant) located in the cathedral containing 18 interface cards each.**
- refresh signals and adjust timing: termination, clock pulse shaping, …
- SVX power management (enable/disable, timed turn on)
- SVX power voltage, current and temperature monitoring
- bias voltage distribution and enable/disable
- stage to next cable run (coax for clocks, 80-conductor 3M for everything else)

Low-mass cable, sub-mini coaxes and adapter card



Interface card



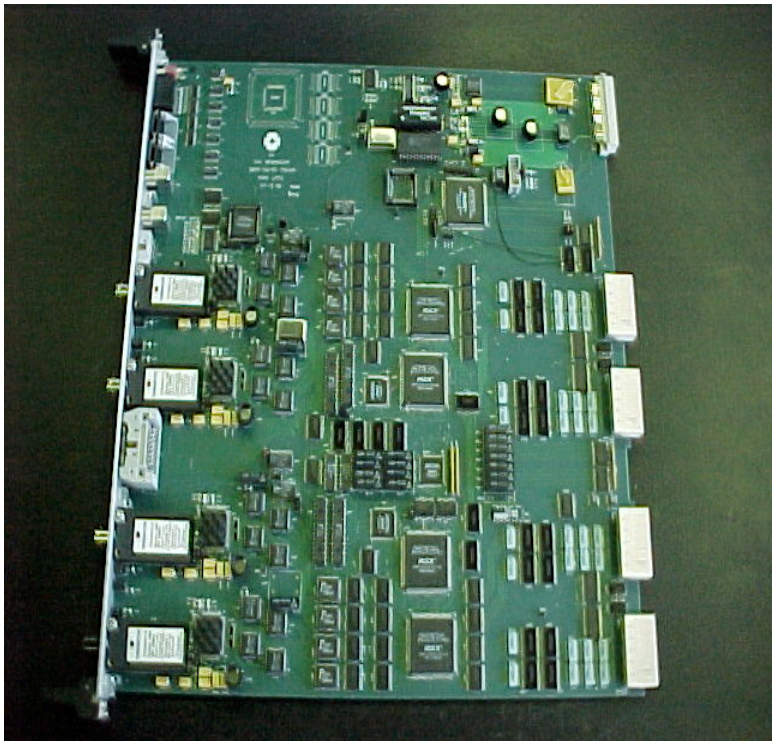

Sequencer Crate
Sequencers
Sequencer Controller
Optical fiber
SCL cable

Individual Readout Components

SEQUENCER

- **6 crates in the platform containing 20 sequencers each.**
- Initialization of the SVX chips in 8 HDIs using the MIL-STD-1553 bus
- Real time manipulation of the SVX control lines to effect data acquisition, digitization and readout based on the NRZ/CLK signals from Sequencer Controller
- Conversion of 8-bit wide SVX readout data to an optical signal operating at 1.062 Gbit/s, sent to the VRB
- ID header and EOR trailer tacked onto data stream. For every HDI the data stream is:

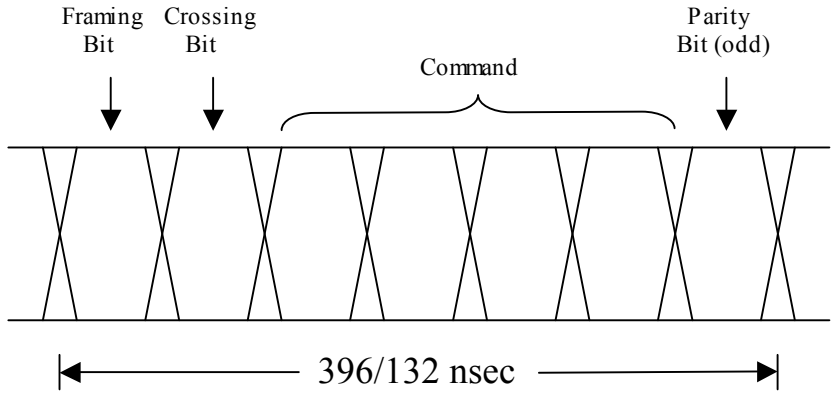
Seq Header	Seq ID	
	Seq Status	
SVX Data	Chip ID	
	Chip Status	
	Channel ID	Channel#0
	Data	
	Channel ID	Channel#1
	Data	
	...	
	Channel ID	Channel#127
	Data	
Seq Trailer	C0	
	C0	



Individual Readout Components

SEQUENCER CONTROLLER

- **One sequencer controller per sequencer crate.**
- Receives the Serial Command Link (SCL): CLK+Trigger decisions
- Generates NRZ based on SCL: continuous stream of 7-bit packet synchronized with the accelerator.



NRZ Command	
IDLE	0000
ACQUIRE	0001
TRIGGER	0011
RAMP	1010
DIGITIZE	0010
READOUT	0110
RESET_PREAMP	0101
CAL_INJECT	0111

VRBC (*VME READOUT BUFFER CONTROLLER*)

- **One VRBC per VRB crate**
- Resides in slot #14 in each of the VRB crates
- Receives the Serial Command Link (SCL): CLK+Trigger decisions
- Performs *handshaking* with the:
  - **VRBs**: prepare the VRB for receiving SVX data via the SVX Sequencer and control the filling and reading of several storage buffers on the VRB
  - **VBD**: coordinate the transmission of the VRB data across the VME backplane to the VBD

Individual Readout Components

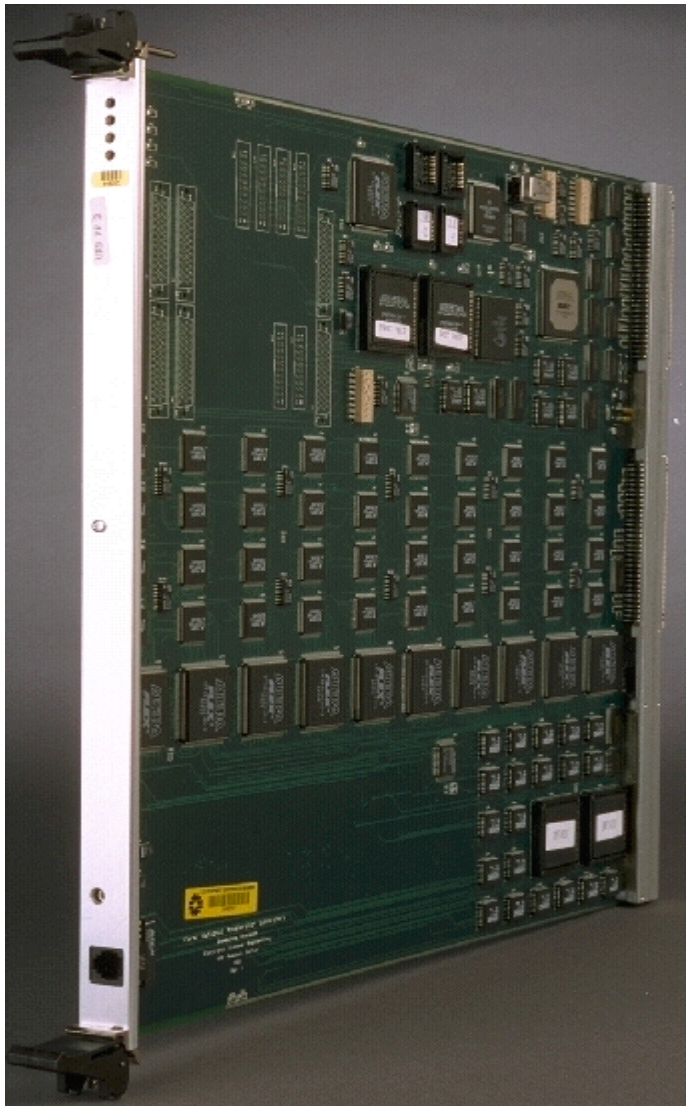
VRB (*VME READOUT BUFFER*)

- **12 crates in MCH2 containing 10 VRBs each.**
- Acts as a buffer for data pending L2 trigger decision
- Receives data via *VME TRANSITION MODULE* (VTM) data link (serial optical connector)
- 8 independent input ports (8 HDIs) and a common VME output port.
- Buffer memory partitioned: 16 x 2 kBytes
- Input data rate ~ 50 Mbytes/sec/channel
- Output data rate ~ 50 Mbytes/sec
- Assumes significant trigger rejection factors between input/output event rates:
  - input @ L1 Accept rate: ~ 5-10 kHz
  - output @ L2 Accept rate: 1 kHz

VBD (*VME BUFFER DRIVER*)

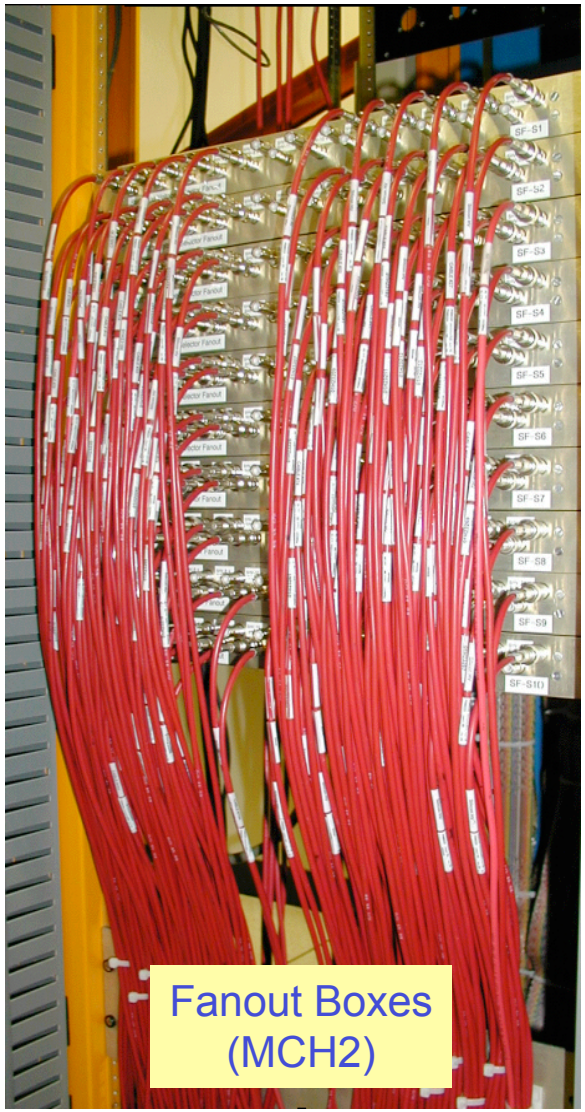
- **One VBD per VRB crate.**
- Serves as the readout device for the VME-based front-end electronics in D0 and output the collected data on a data cable to the L3 farm
- 2 memory buffers (256 kBytes each) in which the data collected from *all* VRBs in the crate (max. 10) is stored

VRB

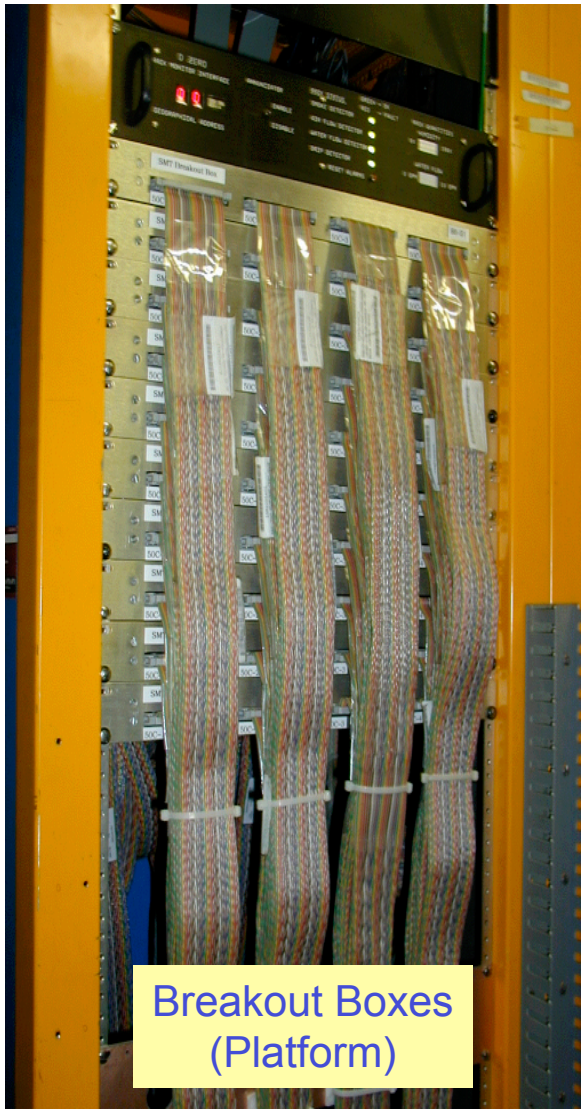


HV Distribution System

HV Modules
(MCH2)



Fanout Boxes
(MCH2)



Breakout Boxes
(Platform)